IN THE CLAIMS:

No claims have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (previously presented) A method of unique sequential marking a plurality of semiconductor devices in a multi-die handling device comprising:
reading an ID code on said multi-die handling device;
retrieving a tray map file corresponding to said ID code;
determining a tray matrix of said multi-die handling device;
retrieving data from the tray map file, said data comprising unique characters correlating to each semiconductor device of said plurality of semiconductor devices; and
marking each semiconductor device with said data.

2. (original) The method according to claim 1, wherein said multi-die handling device comprises a JEDEC tray.

3. (original) The method according to claim 1, wherein said data further comprises non-unique characters.

4. (original) The method according to claim 3, wherein said non-unique characters are selected from the group consisting of semiconductor device data, date code, country code and company logo.

5. (original) The method according to claim 1, wherein said unique characters comprise test data extracted for at least one semiconductor device from the tray map file.

6. (previously presented) The method according to claim 1, wherein each semiconductor device comprises an integrated circuit semiconductor device.

7. (previously presented) The method according to claim 6, wherein said semiconductor device each comprise a semiconductor device selected from the group consisting of Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Single In-Line Memory Modules (SIMMs), and Dual In-Line Memory Modules (DIMMs).

8. (previously presented) The method of claim 1, wherein marking occurs before packaging each semiconductor device.

9. (previously presented) The method of claim 1, wherein marking occurs after packaging each semiconductor device.

10. (previously presented) A method of culling semiconductor devices from a reject bin, said method comprising:
retrieving a plurality of semiconductor devices from at least one reject bin;
providing at least one carrier of a plurality of carriers having a plurality of pocket locations;
assigning said at least one carrier of said plurality of carriers an ID code;
placing each semiconductor device of said plurality of semiconductor devices in a pocket location of said plurality of pocket locations;
testing each semiconductor device;
generating a tray map file comprising test data corresponding to each semiconductor device;
storing the tray map file in association with the ID code of said at least one carrier;
reading the ID code on said at least one carrier;

retrieving the tray map file corresponding to said ID code;
determining a tray matrix of said at least one carrier;
retrieving test data from the tray map file; and
marking each semiconductor device of said plurality of semiconductor devices with the corresponding test data.

11. (original) The method according to claim 10, wherein said carrier is a multi-die handling device.

12. (original) The method according to claim 11, wherein said multi-die handling device comprises a JEDEC tray.

13. (original) The method according to claim 10, wherein said test data comprises non-unique characters.

14. (original) The method according to claim 13, wherein said non-unique characters comprise non-unique characters selected from the group consisting of semiconductor device data, date code, country code and company logo.

15. (previously presented) The method according to claim 10, wherein said semiconductor device each comprise a semiconductor device selected from the group consisting of Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Single In-Line Memory Modules (SIMMs) and Dual In-Line Memory Modules (DIMMs).

16. (original) The method of claim 10, wherein marking occurs before packaging each semiconductor device.

17. (original) The method of claim 10, wherein marking occurs after packaging each semiconductor device.

18. (original) A method of unique sequential marking comprising:
providing a multi-die handling device having a plurality of pockets therein in a matrix;
placing at least one semiconductor device in at least one pocket of said multi-die handling device;
reading an ID code on said multi-die handling device;
retrieving a tray map file corresponding to said ID code;
determining a tray matrix of said multi-die handling device;
retrieving data from the tray map file, said data comprising unique characters correlating to said at least one semiconductor device; and
marking said at least one semiconductor device with said data.

19. (original) The method according to claim 18, wherein said multi-die handling device comprises a JEDEC tray.

20. (original) The method according to claim 18, wherein said data further comprises non-unique characters.

21. (original) The method according to claim 20, wherein said non-unique characters comprise non-unique characters selected from the group consisting of semiconductor device data, date code, country code and company logo.

22. (previously presented) The method according to claim 18, wherein said unique characters comprise test data extracted from said tray map file.

23. (previously presented) The method according to claim 18, wherein said at least one semiconductor device is an integrated circuit semiconductor device.

24. (previously presented) The method according to claim 23, wherein said semiconductor device each comprise a semiconductor device selected from the group consisting of Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Single In-Line Memory Modules (SIMMs), and Dual In-Line Memory Modules (DIMMs).

25. (previously presented) (The method of claim 18, wherein marking occurs before packaging said at least one semiconductor device.

26. (previously presented) The method of claim 18, wherein marking occurs after packaging said at least one semiconductor device.

27. (previously presented) A method of culling semiconductor devices from a reject bin, said method comprising:

retrieving a plurality of semiconductor devices from a reject bin;

providing a plurality of carriers, each carrier having a plurality of pocket locations in a tray matrix;

assigning each carrier of said plurality of carriers an ID code;

placing each semiconductor device of said plurality of semiconductor devices in a pocket location of said plurality of pocket locations;

testing each semiconductor device;

generating a tray map file comprising test data corresponding to each semiconductor device;

storing the tray map file in association with the ID code of each carrier;

reading the ID code on a carrier;

retrieving the tray map file corresponding to said ID code;
determining a tray matrix of the carrier;
retrieving test data from the tray map file; and
marking each semiconductor device of said plurality of semiconductor devices with the corresponding test data.

28. (original) The method according to claim 27, wherein said carrier comprises a multi-die handling device.

29. (original) The method according to claim 28, wherein said multi-die handling device comprises a JEDEC tray.

30. (original) The method according to claim 27, wherein said test data comprises non-unique characters.

31. (original) The method according to claim 30, wherein said non-unique characters comprise non-unique characters selected from the group consisting of semiconductor device data, date code, country code and company logo.

32. (previously presented) The method according to claim 27, wherein said semiconductor device each comprise a semiconductor device selected from the group consisting of Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Single In-Line Memory Modules (SIMMs), and Dual In-Line Memory Modules (DIMMs).

33. (original) The method of claim 27, wherein marking occurs before packaging each semiconductor device.

34. (original) The method of claim 27, wherein marking occurs after packaging each semiconductor device.